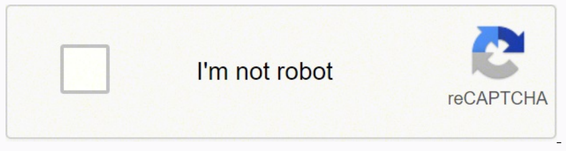

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Introduction MOS Fabrication MOS Transistor Theory and Models MOS Models and IV characteristics MOS Inverters: Static Characteristics and Performance MOS Inverters: Dynamic Characteristics and Performance Combinational Logic Types (CMOS, Ratioed, Pass) and Performance Sequential Logic Dynamic Logic VLSI design and Scaling Memory Design I/O Circuits and Inductive Noise CLK Generation Robust VLSI Design for Variation See Fall 2021 course calendar for day-by-day calendar with assignments. Handwritten assignments will be accepted, but when specified computer generated figures, graphs and results must be submitted and everything should be still combined into a single PDF and submitted in Canvas. K. The book comprises chapters on MOS transistors, modelling of MOS transistors using spice, MOS inverters, semiconductor memories, Chip input and output circuits and design for testability. T. Kang, and C. Duvvury, Modeling of Electrical Overstress in Integrated Circuits, Kluwer Academic Publishers, 1994. Y.-K. No handwritten work will be accepted or graded on projects. Jan M. This text provides rigorous treatment of basic design concepts with detailed examples. Sriram and S. Sung-Mo “Steve” Kang and Sangho Shin, “Energy-Efficient Memristive Analog and Digital Electronics,” Book Chapter, Advances in Neuromorphic Memristor Science and Applications, Springer, 2012. If a student turns in a late assignment without enough late days, the assignment will not be accepted and will receive a 0. Grading is based on homework assignments, midterm, and projects. Surgical masks and Penn cloth masks are recommended. Lectures Lectures will be held in person and will be recorded and posted in Canvas for student use. Digital Integrated Circuits, A Design Perspective, 2nd edition, Prentice Hall, 2003. CMOS Digital Integrated Circuits Analysis & Design, 4th edition, McGraw Hill, 2014 Neil Weste, David Harris. S. If assignments or exams fall due on a religious holiday, please make arrangements with the instructor to accommodate before the posted due date. CMOS VLSI Design: A Circuits and Systems Perspective, 4th edition, Pearson, 2011. Cmos digital integrated circuits is a comprehensive guide for undergraduate students of computer Science engineering. Each student is expected to do his/her own work -- including developing the details, drawing circuits, performing simulations, and writing the solutions. Errata for text Sung-Mo (Steve) Kang, Yusuf Leblebici, and Chul Woo Kim. Teng and S. Kang, Hot-Carrier Reliability of MOS VLSI Circuits, Kluwer Academic Publishers, 1993. It is the students' responsiblity to keep track of their late days. If there is any uncertainty, please ask. Sriram, “Binary Formulations for Placement and Routing Problems,” book chapter, pp. 151-179, Power Aware Design Methodologies, Kluwer Academic Publishers, 2002. P. Kang and H. Late Assignments All students will receive a total of 4 late days they can use on homework and projects. Course Announcements and Discussion You should enroll in Piazza and it will be a closed class (I.e only those registered for the class can access it). Y. Leblebici and S. Aimed at junior/senior courses offered in electrical engineering and computer science, this book starts with CMOS processing, and then covers MOS transition models, basic CMOS gates, dynamic circuits, memory circuits, BiCMOS circuits, I/O circuits, VLSI design methdologies, design for manufacturability and design for testability. Kang, Computer-Aided Design of Optoelectronic Integrated Circuits and Systems, Prentice-Hall, 1996. Students are responsible for checking posted grades in a timely manner. For the homeworks and projects, you are free to discuss basic strategies and approaches with your fellow classmates or others, but detail designs, implementations, analysis, and writeups should always be the work of the individual. Kim, CMOS Digital Integrated Circuits: Analysis and Design, McGraw-Hill, 4th Ed., 2014 Chapters in books S. Grade Adjustment Regrade requests must be submitted to the TA no later than 1 week after the assignment grades are released to the students. J. Morikuni and S. Leblebici, and C. Piazza will be used for all course announcements and discussions. 1375-1391, The Circuits and Filters Handbook, CRC/IEEE Press, 1995. W. J. This book is indispensable for engineering students preparing for GATE and IES. Kang and M. Y. Wu, I. Cheng, C.-H. Unauthorized sharing or recording is a violation of the Code of Academic Integrity. 57-105. Shu, “Automatic Circuit Synthesis Using Switching Network Logic and Metal-Metal Matrix Layout,” book chapter, Advances in Computer-Aided Engineering Design, JAI Press , Inc., 1990, pp. 107-157. Kang, Design Automation for Timing-Driven Layout Synthesis, Kluwer Academic Publishers, 1993. Kang, Electrothermal Analysis of VLSI Systems, Kluwer Academics, June 2000. It addresses both design concepts and computer aided analysis for most of the circuit examples. Homework Assignments [25%] Project 1 [20%] Project 2 [30%] Midterm [25%] Lecture Mask Policy Masks are required to attend lecture in person, and all students are responsible for bringing their own masks. Chen, “Circuit Optimization for CMOS VLSI,” book chapter, Advances in Computer-Aided Engineering Design, JAI Press, Inc., 1990, pp. Books S. Absentees Use the Penn Course Absence Report (CAR) in Penn-in-Touch to report absences. M. Illegible submissions will not be graded. You can find the link above and in Canvas. Apply their course knowledge and the Cadence VLSI CAD tools in two design projects that involve much the same design flow they would encounter in a semiconductor design industrial setting. Kang, and W. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic. There are no regrades on final exams and final projects. In general, you are expected to abide by Penn's Code of Academic Integrity. You are also not allowed to record class sessions yourselves. Projects are presented in formal reports and submission of CAD libraries for verification. Leblebici, CMOS Digital Integrated Circuits: Analysis and Design, McGraw-Hill, Third Ed., 2002. H. S. Sapatnekar and S. Kim and Sung-Mo (Steve) Kang, “Signal Integrity Effects in Custom IC and ASIC Designs,” Raminderpal Singh (editor), IEEE Press, Piscataway NJ and Wiley-Interscience (John Wiley & Sons, Inc.), New York NY, 2002. Previous Offerings Gee, M. Collaboration You may help each other understand how to use the CETS computers and course CAD tools. Kang, Physical Design for Multichip Modules, Kluwer Academic Publishers, 1994. Diaz, S. Chulwoo Kim and Sung-Mo (Steve) Kang, “Low Power Flip-Flop and Clock Network Design Methodologies in High-Performance System-on-a-Chips (SoCs),” book chapter, pp. Kang and Y. Leblebici, CMOS Digital Integrated Circuits: Analysis and Design, McGraw-Hill, 1995. Kang, Y. Assignments turned within 24 hours after the due date is counted as 1 day, within 48 hours is counted as 2 days, and so on. In addition, the book consists of several detailed examples and circuit examples for the students to understand the concepts better. C. Assignment Turnin Homework writeups will be due on select days indicated on the course calendar at midnight and must be uploaded into Canvas as a single PDF. If you get advice or insights from others that influenced your work in any way, please acknowledge this in your writeups. Hajj, S. Kang and Y. N. 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These recordings, as well as previously recorded lectures and other course materials, are made available solely for your personal, educational use and may not be shared, copied or redistributed without the permission of Penn and the instructor. Homeworks must be legible and all work should be shown. Any student coming to class without a mask will be asked to leave and reported to the Office of Student Conduct (OSC). Kang and A. Dharchoudhury, “Modeling of Circuit Performances,” book chapter, pp. This text is the most comprehensive book on the market for CMOS circuits.

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